WHAT IS CLAIMED IS

1. A semiconductor memory comprising:

a first memory array having a plurality of first main word lines, a plurality of sets of first sub word lines, a plurality of pairs of first data lines, and a plurality of first memory cells each of which is coupled to a corresponding one of said plurality of first sub word lines and a corresponding one of said plurality of first data lines, each of said sets of first sub word lines corresponding to one of said plurality of first main word lines;

a second memory array having a plurality of second main word lines, a plurality of sets of second sub word lines, a plurality of pairs of second data lines, and a plurality of second memory cells each of which is coupled to a corresponding one of said plurality of second sub word lines and a corresponding one of said plurality of second data lines, each of said sets of second sub word lines corresponding to one of said plurality of second main word lines;

a third memory array having a plurality of third main word lines, a plurality of sets of third sub word lines, a plurality of pairs of third data lines, and a plurality of third memory cells each of which is coupled to a corresponding one of said plurality of third sub

word lines and a corresponding one of said plurality of third data lines, each of said sets of third sub word line corresponding to one of said plurality of third main word lines;

a fourth memory array having a plurality of fourth main word lines, a plurality of sets of fourth sub word lines, a plurality of pairs of fourth data lines, and a plurality of fourth memory cells each of which is coupled to a corresponding one of said plurality of fourth sub word lines and a corresponding one of said plurality of fourth data lines, each of said sets of fourth sub word lines corresponding to one of said plurality of fourth main word lines;

a pair of first sub common data line extending in a first direction;

a pair of second sub common data line extending in said first direction;

a pair of third sub common data line extending in said first direction;

a pair of fourth sub common data line extending in said first direction;

a pair of first main common data line extending in a second direction perpendicular to said first direction;

a pair of second main common data line extending in said second direction;

a first switching circuit coupled between said plurality of pairs of first data lines and said pair of first sub common data line;

a second switching circuit coupled between said plurality of pairs of second data lines and said pair of second sub common data line;

a third switching circuit coupled between said plurality of pairs of third data lines and said pair of third sub common data line;

a fourth switching circuit coupled between said plurality of pairs of fourth data lines and said pair of fourth sub common data line;

a fifth switching circuit coupled between said pair of first sub common data line and said pair of first main common data line;

a sixth switching circuit coupled between said pair of second sub common data line and said pair of second main common data line;

a seventh switching circuit coupled between said pair of third sub common data line and said pair of first main common data line; and

an eighth switching circuit coupled between said pair of fourth sub common data line and said pair of second main common data line.

2. A semiconductor memory comprising:

a first region extending in a first direction;

a second region extending in said first direction and in parallel with said first region;

a third region extending in a second direction perpendicular to said first direction;

a fourth region extending in said second direction and in parallel with said third region;

a fifth region formed as a rectangle of which three sides are contiguous to said first region, said third region and said fourth region;

a sixth region formed as a rectangle of which two sides are contiguous to said first region and said fourth region;

a seventh region formed as a rectangle of which four sides are contiguous to said first region, said second region, said third region and said fourth region; and

an eighth region formed as a rectangle of which three sides are contiguous to said first region, said second region and said fourth region;

wherein said first region includes a pair of first sub common data line extending in said first direction and a pair of second sub common data line extending in said first direction,

wherein said second region includes a pair of third sub common data line extending in said first direction and a pair of fourth sub common data line extending in said first direction,

wherein said third region includes a pair of first main common data line extending in said second direction,

wherein said fourth region includes a pair of second main common data line extending in said second direction,

wherein said fifth region includes:

(1) a first memory array having a plurality of first word lines, a plurality of pairs of first data lines, and a plurality of first memory cells connected to said plurality of first word lines and said plurality of pairs of first data lines;

(2) a first sense amplifier connected to said plurality of pairs of first data lines; and

(3) a first switching circuit connected interposingly between said plurality of pairs of first data lines and said pair of first sub common data line,

wherein said sixth region includes:

(1) a second memory array having a plurality of second word lines, a plurality of pairs of second data lines, and a plurality of second memory cells connected to said plurality of second word lines and said plurality of pairs of second data lines;

(2) a second sense amplifier connected to said plurality of pairs of second data lines; and

(3) a second switching circuit connected interposingly between said plurality of pairs of second data lines and said pair of second sub common data line,

wherein said seventh region includes:

(1) a third memory array having a plurality of third word lines, a plurality of pairs of third data lines, and a plurality of third memory cells connected to said plurality of third word lines and said plurality of pairs of third data lines;

(2) a third sense amplifier connected to said plurality of pairs of third data lines; and

(3) a third switching circuit connected interposingly between said plurality of pairs of third data lines and said pair of third sub common data line,

wherein said eighth region includes:

(1) a fourth memory array having a plurality of fourth word lines, a plurality of pairs of fourth data lines,

and a plurality of fourth memory cells connected to said plurality of fourth word lines and said plurality of pairs of fourth data lines;

(2) a fourth sense amplifier connected to said plurality of pairs of fourth data lines; and

(3) a fourth switching circuit connected interposingly between said plurality of pairs of fourth data lines and said pair of fourth sub common data line,

wherein said first region and said third region intersect in a region including:

(1) a fifth switching circuit connected interposingly between said pair of first sub common data line and said first main common data line; and

(2) a sixth switching circuit for supplying said first sense amplifier with a supply voltage and a reference voltage,

wherein said first region and said fourth region intersect in a region including:

(1) a seventh switching circuit connected interposingly between said pair of second sub common data line and said second main common data line; and

(2) an eighth switching circuit for supplying said second sense amplifier with said supply voltage and said reference voltage,

wherein said second region and said third region intersect in a region including:

(1) a ninth switching circuit connected interposingly between said pair of third sub common data line and said first main common data line; and

(2) a tenth switching circuit for supplying said third sense amplifier with said supply voltage and said reference voltage, and

wherein said second region and said fourth region intersect in a region including:

(1) an eleventh switching circuit connected interposingly between said pair of fourth sub common data line and said second main common data line; and

(2) a twelfth switching circuit for supplying said fourth sense amplifier with said supply voltage and said reference voltage.

3. A semiconductor memory comprising:

a first memory array having a plurality of first word lines, a plurality of pairs of first data lines, and a plurality of first memory cells connected to said plurality of first word lines and said plurality of pairs of first data lines;

a second memory array having a plurality of second word lines, a plurality of pairs of second data lines,

and a plurality of second memory cells connected to said plurality of second word lines and said plurality of pairs of second data lines;

a third memory array having a plurality of third word lines, a plurality of a pairs of third data lines, and a plurality of third memory cells connected to said plurality of third word lines and said plurality of pairs of third data lines;

a fourth memory array having a plurality of fourth word lines, a plurality of pairs of fourth data lines, and a plurality of fourth memory cells connected to said plurality of fourth word lines and said plurality of pairs of fourth data lines;

a pair of first sub common data line extending in a first direction;

a pair of second sub common data line extending in said first direction;

a pair of third sub common data line extending in said first direction;

a pair of fourth sub common data line extending in said first direction;

a pair of first main common data line extending in a second direction perpendicular to said first direction;

a pair of second main common data line extending in said second direction;

a first switching circuit connected interposingly between said plurality of pairs of first data lines and said pair of first sub common data line;

a second switching circuit connected interposingly between said plurality of pairs of second data lines and said pair of second sub common data line;

a third switching circuit connected interposingly between said plurality of pairs of third data lines and said pair of third sub common data line;

a fourth switching circuit connected interposingly between said plurality of pairs of fourth data lines and said pair of fourth sub common data line;

a first transmission circuit connected interposingly between said pair of first sub common data line and said pair of first main common data line, said first transmission circuit receiving first signals on said pair of first sub common data line and outputting second signals to said pair of first main common data line, said second signals being amplified signals of said first signals;

a second transmission circuit connected interposingly between said pair of second sub common data line and said pair of second main common data line,

said second transmission circuit receiving third signals on said pair of second sub common data line and outputting fourth signals to said pair of second main common data line, said fourth signals being amplified signals of said third signals;

a third transmission circuit connected interposingly between said pair of third sub common data line and said pair of first main common data line, said third transmission circuit receiving fifth signals on said pair of third sub common data line and outputting sixth signals to said pair of first main common data line, said sixth signals being amplified signals of said fifth signals; and

a fourth transmission circuit connected interposingly between said pair of fourth sub common data line and said pair of second main common data line, said fourth transmission circuit receiving seventh signals on said pair of fourth sub common data line and outputting eighth signals to said pair of second main common data line, said eighth signals being amplified signals of said seventh signals.

4. A semiconductor memory comprising:

a plurality of sub-memory mats, each of said sub-memory mats including: a memory array having sub-word

lines and sub-bit lines intersecting orthogonally and dynamic memory cells located in lattice fashion at the intersection points between the intersecting sub-word and sub-bit lines; a sub-word line driver including unit sub-word line driving circuits corresponding to said sub-word lines; a sense amplifier including unit amplifier circuits and column selection switches corresponding to said sub-bit lines; and sub-common I/O lines to which the designated sub-bit lines are connected selectively via said column selection switches, wherein said sub-memory mats are arranged in lattice fashion;

a plurality of main word lines and column selection signal lines intersecting orthogonally above said sub-memory mats; and

a plurality of main common I/O lines to which the designated sub-common I/O lines are connected selectively.

5. A semiconductor memory according to claim 4, wherein said unit sub-word line driving circuits are furnished alternately on both sides of said sub-word lines, said unit sub-word line driving circuits having a pitch twice that of said sub-word lines; and

wherein said unit amplifiers and said column selection switches are provided alternately on both sides of said sub-bit lines, said unit amplifiers and said column selection switches having a pitch twice that of said sub-bit lines.

6. A semiconductor memory according to claim 5, wherein said unit sub-word line driving circuits are shared alternately by the corresponding sub-word lines of two adjacent sub-memory mats located in the column direction; and

wherein said unit amplifiers and said column selection switches are shared alternately by the corresponding sub-bit lines of two adjacent sub-memory mats located in the row direction.

7. A semiconductor memory according to claim 6, wherein said main word lines have a pitch X times that of said sub-word lines, said semiconductor memory further comprising X bits of sub-word line driving signal lines intersecting said main word lines orthogonally, said sub-word line driving circuits selectively placing into selected status the corresponding sub-word lines in accordance with a row selection signal sent via the corresponding main word

lines as well as in accordance with a sub-word line driving signal transmitted via the corresponding sub-word line driving signal lines.

8. A semiconductor memory according to claim 7, wherein each of said unit sub-word line driving circuits is a CMOS static driving circuit comprising: a p-channel first MOSFET which is furnished interposingly between the sub-word line driving signal line and the corresponding sub-word line and of which the gate is connected to an inverted signal line of the corresponding main word line; an n-channel second MOSFET which is furnished interposingly between the corresponding sub-word line and a grounding potential and of which the gate is connected to an inverted signal line of said corresponding main word line; and an n-channel third MOSFET which is furnished in parallel with said first MOSFET and of which the gate is connected to an uninverted signal line of said corresponding main word line.

9. A semiconductor memory according to claim 8, wherein said column selection signal lines have a pitch Y times that of said sub-bit lines, said semiconductor memory further comprising Y sets of said sub-common I/O

lines corresponding to said sub-memory mats, said column selection switches being turned on selectively Y switches at a time in accordance with a column selection signal transmitted via the corresponding column selection signal lines.

10. A semiconductor memory according to claim 9, wherein said sub-common I/O lines are connected selectively to said main common I/O lines via sub-main amplifiers located in a region in which said sub-word line drivers and said sense amplifiers intersect.

11. A semiconductor memory according to claim 10, wherein each of said sub-main amplifiers comprises: a read differential MOSFET of which the gate is connected to the uninverted and inverted signal lines of the corresponding sub-common I/O line and of which the drain is connected to the inverted and uninverted signal lines of the corresponding main common I/O line; and a write switching MOSFET furnished interposingly between the uninverted signal lines as well as between the inverted signal lines of said sub-common I/O lines and said main common I/O lines.

12. A semiconductor memory according to claim 11, wherein said main common I/O lines are furnished in a layer above the region in which said sub-word line drivers are provided, said main common I/O lines intersecting orthogonally with said sub-common I/O lines.

13. A semiconductor memory according to claim 12, wherein said unit amplifiers are fed with operating power via a pair of driving signal lines, said sub-memory mats including sense amplifier driving circuits for selectively transmitting to said driving signal lines said operating power sent from a pair of driving voltage supply lines, said sense amplifier driving circuits being located in a region where said sub-word line drivers and said sense amplifiers intersect.

14. A semiconductor memory according to claim 13, wherein said sense amplifier driving circuits utilize an overdrive scheme whereby said driving signal lines are first supplied with operating power of a relatively large absolute value for a predetermined time and then with operating power of a relatively small absolute value.

15. A semiconductor memory according to claim 14, wherein said semiconductor memory adopts a charge-reused refresh method whereby the operating power transmitted to the driving signal lines of one sense amplifier is forwarded via appropriate switching means to the driving signal lines of the next sense amplifier to be operated.

16. A semiconductor memory according to claim 15, further comprising main bit lines which correspond to the sub-bit lines of a predetermined number of sub-memory mats arranged contiguously in the row direction and to which the sub-bit lines of the designated sub-memory mat are selectively connected, wherein said unit amplifiers of said sense amplifiers and said column selection switches are arranged to correspond with said main bit lines.

17. A semiconductor memory according to claim 16, further comprising a predetermined number of redundant sub-memory mats furnished in the row and the column direction thereof.

18. A semiconductor memory according to claim 17, wherein sense amplifier control signal lines for selectively connecting said driving signal lines to said

driving voltage supply lines are located in a layer above the region in which said sense amplifiers are provided; and

wherein said sub-word line driving signal lines, said main common I/O lines and said driving voltage supply lines are furnished in a layer above the region in which said sub-word line drivers are formed.

19. A semiconductor memory according to claim 18, further comprising three metal wiring layers, wherein said column selection signal lines, said sub-word line driving signal lines, said main common I/O lines and said driving voltage supply lines are formed by the third metal wiring layer which is the highest layer; and

wherein said main word lines, said driving signal lines and said sense amplifier control signal lines are formed by the second metal wiring layer.

20. A semiconductor memory according to claim 19, wherein the layered structure including said main word lines, said driving signal lines, said sense amplifier control signal lines, said column selection signal lines, said sub-word line driving signal lines, said main common I/O lines and said driving voltage supply

lines is patterned without recourse to a phase shift mask scheme.

21. A semiconductor memory according to claim 20, wherein said semiconductor memory is mounted on a p-type semiconductor substrate having data I/O circuits and fed with a relatively small negative potential;

wherein the n-channel MOSFETs constituting part of said memory arrays, said sense amplifiers and said sub-word line drivers are formed in a p-well region of p-type semiconductor substrate;

wherein the n-channel MOSFETs constituting part of peripheral circuits are formed in a p-well region supplied with said grounding potential inside a relatively deep n-well region fed with the supply voltage; and

wherein the n-channel MOSFETs making up part of said data I/O circuits are formed in a p-well region supplied either with said grounding potential or with a negative potential of a relatively large absolute value inside said relatively deep n-well region fed with said supply voltage.

22. A semiconductor memory according to claim 20, wherein said semiconductor memory is mounted on a p-type

semiconductor substrate having data I/O circuits and fed with said grounding potential;

wherein the n-channel MOSFETs constituting part of said memory arrays, said sense amplifiers and said sub-word line drivers are formed in a p-well region fed with a negative potential of a relatively small absolute value inside a relatively deep n-well region supplied with a word line selection potential;

wherein the n-channel MOSFETs making up part of peripheral circuits are formed in a p-well region of said p-type semiconductor substrate; and

wherein the n-channel MOSFETs constituting part of said data I/O circuits are formed in a p-well region supplied either with said grounding potential or with a negative potential of a relatively large absolute value inside a relatively deep n-well region fed with the supply voltage.

23. A semiconductor memory according to claim 20, wherein said semiconductor memory is mounted on a p-type semiconductor substrate having data I/O circuits and fed with said grounding potential;

wherein the n-channel MOSFETs constituting part of said memory arrays and said sub-word line drivers are formed in a p-well region fed with a negative potential

of a relatively small absolute value inside a relatively deep n-well region supplied with a word line selection potential;

wherein the n-channel MOSFETs constituting part of said sense amplifiers and peripheral circuits are formed in a p-well region on said p-type semiconductor substrate; and

wherein the n-channel MOSFETs constituting part of said data I/O circuits are formed in a p-well region supplied either with said grounding potential or with a negative potential of a relatively large absolute value inside a relatively deep n-well region fed with the supply voltage.

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